**Question #1:** What is the difference between Flip-Flop and latch?m

|  |  |
| --- | --- |
| **Latch** | **Flip-Flop** |
| Latch is an electronic logic circuit with two stable states  i.e. it is a bistable multivibrator. Latch has a feedback path to retain the information. Hence a latch can be a memory device. | Flip flop is a sequential circuit which generally samples its inputs and changes its outputs only at particular instants of time and not continuously. Flip flop is said to be edge sensitive or edge triggered rather than being level triggered like latches. |

**Question #2:** What is the difference between synchronous and asynchronous inputs?

|  |  |
| --- | --- |
| **Asynchronous sequential circuit.** | **Synchronous sequential circuit.** |
| If some or all the outputs of a sequential circuit do not change (affect) with respect to active transition of clock signal, then that sequential circuit is called  As **Asynchronous sequential circuit**. | If all the outputs of a sequential circuit change (affect) with respect to active transition of clock signal, then that sequential circuit is called as **Synchronous sequential circuit**. |

**Question #3:** What are the applications of different Flip-Flops?

**Applications of flip flop:**

Application of the flip flop circuit mainly involves in bounce elimination switch, data storage, data transfer, latch, registers, counters, frequency division, memory, etc.

**Question #4:** What is the difference of Edge triggering over level triggering?

|  |  |
| --- | --- |
| **Edge triggering** | **level triggering** |
| If the sequential circuit is operated with the clock signal that is transitioning from Logic Low to Logic High, then that type of triggering is known as **Positive edge triggering**. It is also called as ***rising edge triggering***.  If the sequential circuit is operated with the clock signal that is transitioning from Logic High to Logic Low, then that type of triggering is known as **Negative edge triggering.** It is also called as ***falling edge triggering***. | If the sequential circuit is operated with the clock signal when it is in **Logic High**, then that type of triggering is known as **Positive level triggering**. It is highlighted in below figure.  If the sequential circuit is operated with the clock signal when it is in **Logic Low**, then that type of triggering is known as **Negative level triggering**. It is highlighted in the following figure. |

Diagram, schematic

Description automatically generated**Task #1:** Design a circuit on MultiSim using D Flip Flop?

TruthTable

|  |  |  |
| --- | --- | --- |
| **C** | **D** | **Q** |
| 0 | X | No Change |
| 1 | 0 | Q=0 ; Reset State |
| 0 | 1 | Q=1 ; Set State |

**Task #2:** Design a circuit on MultiSim using SR Flip Flop?

Diagram

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TruthTable

|  |  |  |  |
| --- | --- | --- | --- |
| **C** | **S** | **R** | **Q** |
| 0 | X | X | No Change |
| 1 | 0 | 0 | No Change |
| 1 | 0 | 1 | Q=0 ; Reset State |
| 1 | 1 | 0 | Q=1 ; Set State |
| 1 | 1 | 1 | Indeterminate |

Chart

Description automatically generated**Task #3:** Design a circuit on MultiSim using JK Flip Flop?

|  |  |  |
| --- | --- | --- |
| **J** | **K** | **Q(t + 1)** |
| 0 | 0 | Q(t) |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | Q(t)' |

TruthTable